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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,732	04/14/2004	Eric B. Blecker	1875.2570002/RES/GSB	4788
26111	7590	01/27/2005	EXAMINER	
STERNE, KESSLER, GOLDSTEIN & FOX PLLC 1100 NEW YORK AVENUE, N.W. WASHINGTON, DC 20005			NGUYEN, PATRICIA T	
			ART UNIT	PAPER NUMBER
			2817	

DATE MAILED: 01/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

## Office Action Summary

Application No.

10/823,732

Applicant(s)

BLECKER ET AL.

Examiner

Patricia T Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☐ Responsive to communication(s) filed on \_\_\_\_.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-17 and 19-20 is/are rejected.
- 7) ☒ Claim(s) 18 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_.
- 4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_.

**DETAILED ACTION*****Claim Rejections - 35 USC § 112***

Claims 1-9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Neither shown in the drawings, nor anywhere in the specification that mentions a second differential transistor pair has substrates connected to respective sources of the second differential transistor pair as claimed in claim 1.

***Claim Rejections - 35 USC § 102***

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-8, 10-17, 19-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Kimura, U.S. Patent # 6,657,486 B2.

Figs. 6 and 8 of Kimura discloses an amplifier comprising: In Fig. 6, transistors M1, M2 (PMOS) can be read as a first differential transistor pair; current source Iss (or in Fig. 8 current source M5) can be read as a first tail current source transistor; transistors M3, M4 (PMOS) can be read as a load transistor pair; transistors M5, M6 (PMOS) can be read as a second differential transistor pair; current source  $5/4 I_o$  can be read as a second tail current source transistor; transistor M10 can be read as an output stage. (Note that it

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is well known in the art as shown in Fig. 8 that a tail current source transistor M5 acts as a tail current source  $I_{ss}$  in Fig. 6).

Regarding claim 10, In Fig. 6, the stage having transistors M1, M2 can be read as a first stage and transistors M1, M2 (PMOS) can be read as a second differential transistor pair; current source  $I_{ss}$  (or in Fig. 8 current source M5) can be read as a second tail current source transistor; the stage having transistors M5, M6 can be read as an input stage and transistors M5, M6 (PMOS) can be read as a first differential transistor pair; current source  $5/4 I_o$  (or in Fig. 8 current source M5) can be read as a first tail current source transistor; transistors M3, M4 (PMOS) can be read as a load transistor pair; transistor M10 can be read as an output stage.

Regarding claim 16, in Fig. 8, amplifier A can be read as an amplifier.

#### ***Allowable Subject Matter***

Claims 9 and 18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

#### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Patricia T Nguyen whose telephone number is (703) 308-1927. The examiner can normally be reached on 6:30 AM - 5:00 PM.

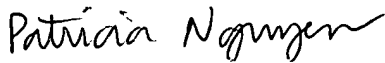
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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on 703-309-4940. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PTN

January 24, 2005



**PATRICIA NGUYEN**  
**PRIMARY EXAMINER**